

AMENDMENTS TO THE DRAWINGS

Attached hereto are two (2) sheets of corrected formal drawings that comply with the provisions of 37 C.F.R. § 1.84. The corrected formal drawings incorporate the following drawing changes:

Figs. 4 and 5 – all references to “CAPS” have been amended to read
“CELL”

It is respectfully requested that the corrected formal drawings be approved and made a part of the record of the above-identified application.



REPLACEMENT SHEET

4/15

- t_0 : WORD LINE LATCHED, ACTIVE PULLDOWN TO 0
- t_1 : BIT LINE CLAMP RELEASED - SENSE AMP ON
- t_2 : BIT LINE DECISION - DATA LATCHED
- t_3 : WORD LINE RETURNED TO QUIESCENT $V_s/2$
- t_4 : WRITE DATA LATCHED ON BIT LINES
- t_5 : WORD LINE PULLED TO V_s - SET/RESET CELL
- t_6 : WORD LINE RETURNED TO QUIESCENT $V_s/2$
- t_7 : BIT LINES ACTIVELY RETURNED TO V_s CLAMP
- t_8 : READ/WRITE CYCLE COMPLETE

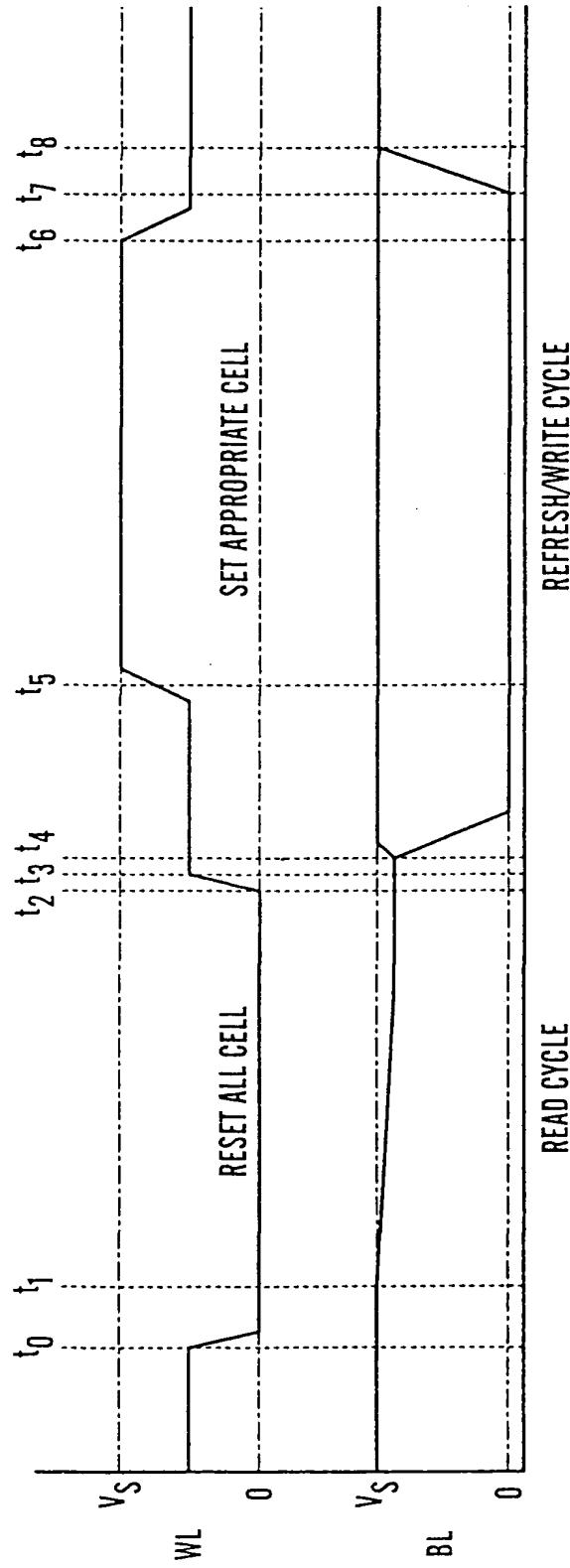
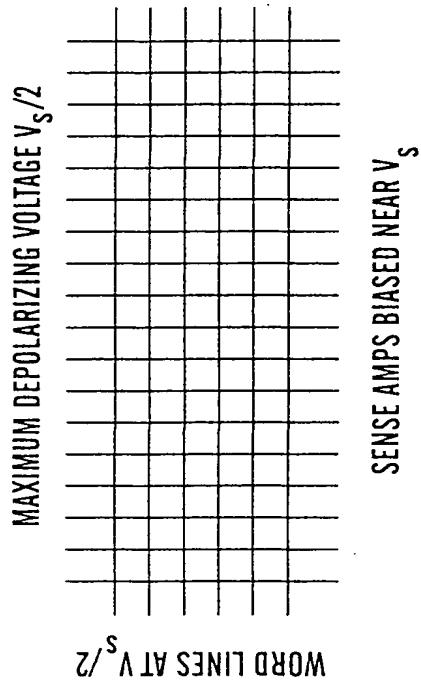


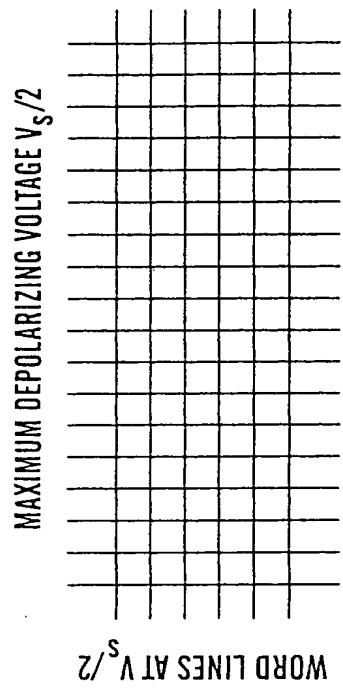
Fig. 4



REPLACEMENT SHEET

5/15

- t_0 : WORD LINE LATCHED, ACTIVE PULL UP TO V_s
- t_1 : BIT LINE CLAMP RELEASED - SENSE AMP ON
- t_2 : BIT LINE DECISION - DATA LATCHED
- t_3 : WORD LINE RETURNED TO QUIESCENT $V_s/2$
- t_4 : WRITE DATA LATCHED ON BIT LINES
- t_5 : WORD LINE PULLED TO 0 - SET/RESET CELL
- t_6 : WORD LINE RETURNED TO QUIESCENT $V_s/2$
- t_7 : WORD LINE ACTIVELY RETURNED TO 0 CLAMP
- t_8 : READ/WRITE CYCLE COMPLETE



SENSE AMPS BIASED NEAR V_s

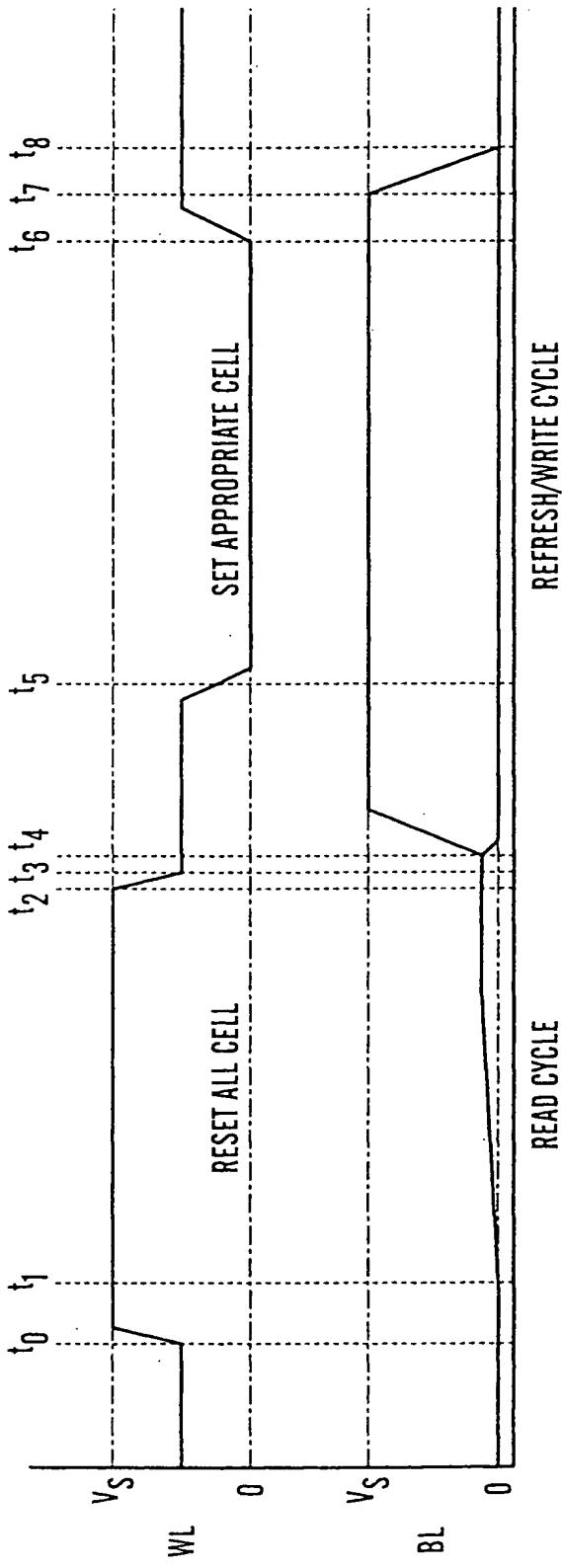


Fig.5